

PATENT
Attorney Docket 4181US (96-973.2)

NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number: EL700255248US

Date of Deposit with USPS: August 31, 2000

Person making Deposit: Amanda Trulson

APPLICATION FOR LETTERS PATENT

for

**METHOD FOR USING DATA REGARDING MANUFACTURING
PROCEDURES INTEGRATED CIRCUITS (IC'S) HAVE UNDERGONE,
SUCH AS REPAIRS, TO SELECT PROCEDURES THE IC'S WILL UNDERGO,
SUCH AS ADDITIONAL REPAIRS**

Inventors:

Salman Akram
Warren M. Farnworth
Derek J. Gochnour
David R. Hembree
Michael E. Hess
John O. Jacobson
James M. Wark
Alan G. Wood

Attorneys:

James R. Duzan
Registration No. 28,393
TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, Utah 84110
(801) 532-1922

**METHOD FOR USING DATA REGARDING MANUFACTURING PROCEDURES
INTEGRATED CIRCUITS (IC'S) HAVE UNDERGONE, SUCH AS REPAIRS, TO
SELECT PROCEDURES THE IC'S WILL UNDERGO, SUCH AS ADDITIONAL
REPAIRS**

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation-in-part of application Serial No. 09/292,655, filed April 15, 1999, now U.S. Patent 6,363,295, issued March 26, 2002, which is a continuation of application Serial No. 08/871,015, filed June 6, 1997, now U.S. Patent No. 5,907,492, issued May 25, 1999.

[0002] This application is related to: an application having Serial No. 08/591,238, filed January 17, 1996, entitled "METHOD AND APPARATUS [sic] FOR STORAGE OF TEST RESULTS WITHIN AN INTEGRATED CIRCUIT", abandoned in favor of a continuation-in-part application filed February 27, 1998, having Serial No. 09/032,417, and entitled "METHOD AND APPARATUS [sic] FOR STORAGE OF TEST RESULTS WITHIN AN INTEGRATED CIRCUIT", now U.S. Patent 6,194,738, issued February 27, 2001; an application having Serial No. 08/664,109, filed June 13, 1996, entitled "A STRUCTURE AND A METHOD FOR STORING INFORMATION IN A SEMICONDUCTOR DEVICE", now U.S. Patent 5,895,962, issued April 20, 1999; an application filed January 17, 1997 having Serial No. 08/785,353 and entitled "METHOD FOR SORTING INTEGRATED CIRCUIT DEVICES", now U.S. Patent 5,927,512, issued July 27, 1999; an application filed February 17, 1997 having Serial No. 08/801,565 and entitled "METHOD OF SORTING A GROUP OF INTEGRATED CIRCUIT DEVICES FOR THOSE DEVICES REQUIRING SPECIAL TESTING", now U.S. Patent 5,844,803, issued December 1, 1998; an application filed February 26, 1997 having Serial No. 08/806,442 and entitled "METHOD IN AN INTEGRATED CIRCUIT (IC) MANUFACTURING PROCESS FOR IDENTIFYING AND RE-DIRECTING IC'S MIS-PROCESSED DURING THEIR MANUFACTURE", now U.S. Patent 5,915,231, issued June 22, 1999; and an application filed March 24, 1997 having Serial No. 08/822,731 and entitled

“METHOD FOR CONTINUOUS, NON LOT-BASED INTEGRATED CIRCUIT MANUFACTURING”, now U.S. Patent 5,856,923, issued January 5, 1999.

BACKGROUND OF THE INVENTION

[0003] Field of the Invention: The present invention relates in general to integrated circuit semiconductor device (IC) manufacturing. More specifically, it relates to methods in IC manufacturing processes for using data regarding manufacturing procedures IC's have undergone, such as repair procedures, to select procedures the IC's will undergo, such as additional repair procedures.

[0004] State of the Art: As shown in FIG. 1, a typical process 10 for manufacturing very small electronic semiconductor device circuits referred to as “Integrated Circuits” (IC's) begins with the IC's being formed or “fabricated” on the surface of a wafer 12 of semiconductor material, such as silicon. Once fabricated, IC's are electronically probed to determine whether they are functional (i.e., “good”) or nonfunctional (i.e., “bad”). If any IC's are found to be bad, an attempt is made to repair those IC's by replacing nonfunctional circuit elements in the IC's with spare circuit elements. For example, Dynamic Random Access Memory (DRAM) IC's are typically repaired by replacing nonfunctional rows or columns of memory cells in the IC's with spare rows or columns.

[0005] These repairs are not always successful, because the number of spare circuit elements on an IC may be exhausted before all nonfunctional circuit elements on the IC are replaced, and because some circuit elements on IC's have no spares to replace them. As a result, a number of bad IC's typically remain on a wafer 12 even after attempts are made to repair the IC's. The location of bad IC's on a wafer 12, along with the location of any good IC's on the wafer 12, is typically stored in a computer database commonly referred to as a “wafer map.”

[0006] After being probed and, if necessary, repaired, IC's begin an assembly process with their wafer 12 being mounted on an adhesive film. In some instances, the film is a special high-adhesion Ultraviolet (U.V.) film. Without cutting the adhesive film, IC's are sawed from their wafer 12 into discrete IC dice or “chips” using high-speed precision dicing equipment. IC dice mounted on U.V. film are then exposed to U.V. light to loosen the grip of the film on the

dice. IC dice identified as good by their wafer map are then each “picked” by automated equipment from their sawed wafer 12 and its associated film and “placed” on an epoxy-coated bonding site of one lead frame in a strip of interconnected lead frames, while IC dice identified as bad are discarded into a scrap bin 14. The epoxy attaching the good IC dice to their lead frames is then cured, and the attached dice are wire bonded to their lead frames using high-speed bonding equipment.

[0007] Once wire bonded, IC dice and their associated lead frames are formed into IC packages using a hot thermosetting plastic encapsulant injected into a mold. IC packages are then cured to set their plastic encapsulant. After encapsulation and curing, leads of the lead frames projecting from the packages are dipped in a cleansing chemical bath in a process referred to as “de-flash” and then electroplated with a lead/tin finish. Connections between lead frames in lead frame strips are then cut to “singulate” IC packages into discrete IC devices.

[0008] After assembly, discrete IC devices are tested in a simple electronic test referred to as an “opens/shorts” test, which checks for “opens” (i.e., no connection) within the devices where connections should exist and “shorts” (i.e., a connection) where connections should not exist. Devices that pass the opens/shorts test proceed on through the process 10 to various burn-in and test procedures where they are tested for functionality, operability, and reliability, and devices that pass these burn-in and test procedures are then typically shipped to customers.

[0009] IC devices that fail any of the opens/shorts, burn-in, and test procedures are checked to determine whether they are repairable. This “check” typically includes an electronic “querying” of a device to determine whether enough spare circuit elements remain in the device to effect necessary repairs. Devices determined to be unrepairable are scrapped in a scrap bin 16, while devices that are repairable are repaired, typically by replacing nonfunctional circuit elements in the devices with spare circuit elements in the same manner as described above. After being repaired, these devices then reenter the manufacturing process 10 just prior to the opens/shorts, burn-in, or test procedures they failed.

[0010] Electronic querying of IC devices to determine whether spare circuit elements are available to effect repairs increases the time required to move the devices through the manufacturing process 10 and places an additional burden on expensive testing resources. While

the extra time added by querying one IC device may be insignificant, the time required to query thousands and thousands of IC devices adds up and can result in a significant reduction in the number of IC devices completing the manufacturing process 10 in a given amount of time. Therefore, there is a need in the art for a method of determining whether enough spare circuit elements are available in an IC device to effect repairs without having to query the device.

[0011] Similarly, as shown in FIG. 2, a typical process 20 for manufacturing so-called “flip-chip” and “Chip-On-Board” (COB) Multi-Chip Modules (MCM's), in which multiple IC dice are typically attached directly to a substrate, such as a printed circuit board (PCB), begins with IC's being fabricated on the surface of a semiconductor wafer 22 in the same manner as described above. Once fabricated, IC's are electronically probed to determine whether they are good or bad, and if any IC's are found to be bad, an attempt is made to repair those IC's (i.e., make them good IC's) by replacing nonfunctional circuit elements in the IC's with spare circuit elements. The locations of good and bad IC's on a wafer 22 are then typically stored in an electronic wafer map.

[0012] After being probed and, if necessary, repaired, IC's begin an assembly process with their wafer 22 being mounted on an adhesive film. Without cutting this film, IC's are then sawed from their wafer 22 into discrete IC dice using high-speed precision dicing equipment. IC dice that are mounted on the special high-adhesion U.V. film described above are then exposed to U.V. light to loosen the grip of the film on the dice.

[0013] IC dice identified as good by their electronic wafer map are then each picked by automated equipment from their sawed wafer 22 and its associated film, typically for attachment to a substrate in a panel of multiple substrates, such as a panel of interconnected PCB's. If the assembly process is a flip-chip process, picked dice are then flipped and directly attached at their active, frontside surfaces to substrates to form MCM's. If the assembly process is a COB process, picked dice are directly attached at their inactive, backside surfaces to adhesive-coated bonding sites of substrates to form MCM's. IC dice identified as bad are discarded into a scrap bin 24.

[0014] Panels of MCM's are then cured. If the assembly process is a COB process, the MCM's may be plasma cleaned, if necessary, and the COB IC dice are then wire bonded to their substrates using high-speed bonding equipment.

[0015] After assembly, panels of MCM's are tested in an opens/shorts test. Panels having COB IC dice that pass the opens/shorts test proceed on through the manufacturing process 20 so the dice can be encapsulated using an overmold, hard cover, or so-called "glob" top, while panels having flip-chip IC dice that pass the opens/shorts test may have their dice encapsulated using an underfill followed by an overmold, hard cover, or glob top. As will be described in more detail below, alternatively, flip-chip IC dice may be encapsulated after burn-in and test procedures. The disposition of panels of MCM's having COB and flip-chip attached IC dice that fail the opens/shorts test will be described in more detail below.

[0016] Panels of MCM's having both COB and flip-chip IC dice, including those panels having flip-chip IC dice that were not encapsulated, are then singulated into discrete MCM's, typically by a shear press or router. After singulation, those MCM's having encapsulated IC dice have their dice tested again in an additional opens/shorts test to check for problems caused by the encapsulation. MCM's having encapsulated dice that pass this additional opens/shorts test, as well as MCM's having dice that were not encapsulated, then proceed on in the manufacturing process 20 to various burn-in and test procedures. The disposition of any MCM's having encapsulated dice that fail the additional opens/shorts test will be described in more detail below.

[0017] After the burn-in and test procedures, MCM's having unencapsulated flip-chip IC dice that pass the procedures proceed on in the process 20 so their dice may be covered with an overmold, hardcover, or glob top. Dice covered in this manner are then checked in a further opens/shorts test for problems caused by their being covered, and MCM's having dice that pass this further test are then typically shipped to customers. MCM's having encapsulated IC dice that pass the burn-in and test procedures skip this final opens/shorts test and typically proceed to shipping.

[0018] MCM's having attached IC dice that fail any of the opens/shorts, burn-in, and test procedures are checked to determine whether their associated IC dice are repairable. This "check" typically includes an electronic querying of the IC dice to determine whether enough

spare circuit elements remain in the dice for effecting repairs. MCM's determined to have unrepairable IC dice are then either reworked using replacement IC dice in an expensive and time-consuming procedure or scrapped in a scrap bin 26, while MCM's having IC dice that are repairable are repaired, typically by replacing nonfunctional circuit elements in the IC dice with spare circuit elements. After being repaired, these MCM's then reenter the manufacturing process 20 just prior to the opens/shorts, burn-in, or test procedures they failed.

[0019] As discussed above, electronic querying of IC dice to determine whether spare circuit elements are available to effect repairs increases the time required to move MCM's through the manufacturing process 20 and places an additional burden on expensive testing resources. Also, IC dice that require repair, and are found to be unrepairable only after the assembly process, waste assembly time, materials, and resources and necessitate the scrapping or reworking of MCM's that may contain many functional dice. It is desirable, then, to have an IC manufacturing method for identifying unrepairable IC dice so they may be kept out of COB, flip-chip, and other MCM assembly processes.

[0020] As described in U.S. Patent No.'s 5,301,143, 5,294,812, and 5,103,166, some methods have been devised to electronically identify IC dice. Such methods take place "off" the manufacturing line, and involve the use of electrically retrievable identification (ID) codes, such as so-called "fuse ID's," programmed into individual IC dice to identify the dice. The programming of a fuse ID typically involves selectively blowing an arrangement of fuses or anti-fuses in an IC die using electric current or a laser so that when the fuses or anti-fuses are accessed, they output a preprogrammed ID code. Unfortunately, none of these methods addresses the problem of identifying unrepairable IC dice "on" a manufacturing line.

SUMMARY OF THE INVENTION

[0021] The present invention provides a method in an integrated circuit (IC) manufacturing process for using data regarding manufacturing procedures IC's have undergone, such as repair procedures at probe, to select manufacturing procedures the IC's will undergo, such as additional repair procedures during back-end testing. The IC's are each programmed with a substantially unique identification (ID) code, such as a fuse ID.

[0022] The method includes storing data in association with the ID codes of the IC's that identifies manufacturing procedures the IC's have undergone. This data may identify spare circuitry already used to repair the IC's at probe, for example, or spare circuitry available to repair the IC's. The ID codes of the IC's are automatically read, for example, at an opens/shorts test during the manufacturing process. The data stored in association with the ID codes is then accessed, and manufacturing procedures the IC's will undergo, such as additional repair procedures during back-end testing, are selected in accordance with the accessed data. Thus, for example, the accessed data may indicate that insufficient spare circuitry is available on an IC to effect repairs, so the IC can proceed directly to a scrap bin without being "queried" to determine the availability of spare circuitry, as is traditionally necessary. The present invention thus eliminates the time-wasting conventional process of querying IC's prior to repair or scrapping.

[0023] Further embodiments include methods of manufacturing IC devices and Multi-Chip Modules (MCM's) which incorporate the method described above.

[0024] In an additional embodiment, a method in an MCM manufacturing process for diverting good but unrepairable IC dice from the process includes storing data in association with ID codes, such as fuse ID's, of the IC's that identifies IC's that are a) good and repairable, b) good but unrepairable, and c) bad. In the inventive method, the ID codes of the IC's are automatically read, and the data stored in association with the ID codes is accessed. IC's identified as good but unrepairable by the accessed data are diverted to other IC manufacturing processes, while IC's identified as bad are discarded, and IC's identified as good and repairable are assembled into MCM's.

[0025] The present invention thus prevents IC's that are unrepairable from being assembled into MCM's, such as Single In-Line Memory Modules (SIMM's), and thus prevents the reworking or scrapping of MCM's into which unrepairable IC's have been assembled.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0026] FIG. 1 is a flow diagram illustrating a conventional integrated circuit (IC) device manufacturing process;

[0027] FIG. 2 is a flow diagram illustrating a conventional Chip-On-Board (COB) or flip-chip attached IC manufacturing process;

[0028] FIG. 3A is a flow diagram illustrating an IC device manufacturing process in accordance with the present invention;

[0029] FIG. 3B is a flow diagram illustrating an assembly portion of the manufacturing process of FIG. 3A in more detail;

[0030] FIG. 4A is a flow diagram illustrating a COB or flip-chip multi-chip module IC manufacturing process in accordance with the present invention; and

[0031] FIG. 4B is a flow diagram illustrating an assembly portion of the manufacturing process of FIG. 4A in more detail.

DETAILED DESCRIPTION OF THE INVENTION

[0032] As shown in FIG. 3A, an inventive process 30 for manufacturing Dynamic Random Access Memory (DRAM) Integrated Circuit semiconductor devices (IC's) begins with DRAM IC's being fabricated in a fabrication step 32 on the surface of a semiconductor wafer 34. It will be understood by those having skill in the field of this invention that the present invention is applicable to any IC devices, including Static Random Access Memory (SRAM) IC's, Synchronous DRAM (SDRAM) IC's, processor IC's, Single In-line Memory Modules (SIMM's), Dual In-line Memory Modules (DIMM's), Rambus In-Line Memory Modules (RIMM), Small Outline Rambus In-Line Memory Modules (SO-RIMM), Personal Computer Memory Format (PCMCIA), Board-Over-Chip type substrate configurations, and other Multi-Chip Modules (MCM's). It will also be understood that although the present invention will be described below in the context of a wire bond/lead frame assembly process, either a conventional lead frame or leads-over-chip configuration using adhesive tape on the lead frame or the semiconductor die or non-conductive adhesive on the active surface of the semiconductor die (LOC), the present invention is applicable to any IC assembly process, including, for example, Chip On Board (COB)-either single semiconductor device or the modular form of multiple semiconductor device IC's, Board Over Chip (BOC)-either single semiconductor device or the modular form of multiple semiconductor device IC's, any configuration of substrate and component including

Tessera style electrical components (film on elastomer), flip-chip processes (as will be described below with respect to FIG.'s 4A and 4B), Tape-Automated Bonding (TAB) processes, and wafer scale semiconductor device packages or packaging, either the entire wafer as a whole, multiple semiconductor devices as portions of the wafer which are singulated and packaged, or the singulation of the semiconductor devices on the wafer which are later packaged and/or mounted.

[0033] Once fabricated, the DRAM IC's are electronically probed in a probe step 36 to determine whether they are good or bad, and if any DRAM IC's are found to be bad, an attempt is made to repair those IC's by replacing nonfunctional rows or columns in the IC's with spare rows or columns. The location of bad DRAM IC's on a wafer 34, along with the location of any good DRAM IC's on the wafer 34, is stored in a computer in an electronic wafer map in association with data identifying spare rows and columns still available in each of the DRAM IC's after any repairs performed at the probe step 36. Of course, it will be understood that the stored data may alternatively identify spare rows and columns used in each of the DRAM IC's to effect repairs at the probe step 36.

[0034] During the probe step 36, DRAM IC's fabricated on the wafers 34 are programmed in the manner described above with a fuse identification (ID) unique to each IC. The fuse ID for each DRAM IC is then stored in association with the repair data 38 for that IC. The fuse ID may identify, for example, a wafer lot ID, the week the DRAM IC's were fabricated, a wafer ID, a die location on the wafer, and a fabrication facility ID. As a result of storing the fuse ID for each DRAM IC in association with the repair data 38, the availability of spare rows or columns for effecting post-probe repairs in a particular DRAM IC can be determined by using the fuse ID of the IC to access the stored repair data 38 for the IC, as will be described in more detail below.

[0035] It will be understood, of course, that the present invention includes within its scope DRAM IC's and other IC's having any ID code, such as a dot code, bar code, or any suitable type marking code on the IC's, including those having fuse ID's. It will also be understood that the IC's may be programmed with their fuse ID's at steps in the manufacturing process 30 other than the probe step 36.

[0036] After being probed and, if necessary, repaired, DRAM IC's enter an assembly process 40 in which good IC's are assembled into IC devices, as will be described in more detail below with respect to FIG. 3B, while bad IC's are discarded in a scrap bin 42. In addition, DRAM IC's 44 that have been diverted from COB and flip-chip manufacturing process flows enter the assembly process 40 and are also assembled into IC devices. The DRAM IC's 44 are diverted from the COB and flip-chip process flows because so many of their spare rows and columns have been used at probe to effect repairs in the DRAM IC's 44 that the DRAM IC's 44 fall below a minimum threshold level of repairability, as will be described in more detail below with respect to FIG.'s 4A and 4B.

[0037] After the assembly process 40, discrete DRAM IC devices are tested in an opens/shorts test 46. There, the fuse ID of the DRAM IC in each IC device is automatically read and correlated with the repair data 38 produced in the manufacturing process 30 or repair data 48 produced in a COB or flip-chip process flow as described below. It should be understood that although the fuse ID's of DRAM IC's in the process 30 are typically read electronically, they may also be read optically if the fuse ID's consist of "blown" laser fuses that are optically accessible. It should also be understood that the fuse ID's of DRAM IC's may be read at steps in the process 30 other than the opens/shorts test 46.

[0038] DRAM IC devices that pass the opens/shorts test 46 proceed on through the process 30 to various burn-in and test procedures 50 and 52 where they are tested for functionality, operability, and reliability, and DRAM IC devices that pass these burn-in and test procedures 50 and 52 are shipped 54 to customers.

[0039] DRAM IC devices that fail any of the opens/shorts, burn-in, and test procedures 46, 50, and 52 proceed to repair 56. Those DRAM IC devices that do not have enough available spare rows and columns to effect repairs, and thus are unrepairable, are identified as such when their repair data 38 and 48 is accessed at the opens/shorts test 46, and these devices proceed directly to rework or a scrap bin 58 without the need to query them. Of course, DRAM IC devices that are identified by their repair data 38 and 48 as being repairable are repaired, typically by replacing nonfunctional rows and columns with spare rows and columns in the same manner as described above. After being repaired, these DRAM IC devices

then reenter the manufacturing process 30 just prior to the opens/shorts, burn-in, or test procedures 46, 50, and 52 they failed.

[0040] It should be understood, of course, that the present invention is applicable to situations in a wide variety of IC manufacturing processes in which data regarding manufacturing procedures the IC's have undergone, such as repair procedures at probe, may be accessed through the use of fuse ID's and other ID codes to determine procedures the IC's should undergo, such as post-probe repairs.

[0041] As stated above, the assembly process 40 of FIG. 3A is shown in more detail in FIG. 3B. In the process 40, probed and repaired semiconductor wafers enter a wafer saw step 60 and are mounted on an adhesive film. The film may be any one of a wide variety of adhesive films used for this purpose, including, for example, a special high-adhesion U.V. film. Without cutting the film, DRAM IC's are then sawed from their wafer into discrete IC dice using high-speed precision dicing equipment. DRAM IC dice that are mounted on the special high-adhesion U.V. film are then exposed to U.V. light in an optional U.V. exposure step 62 to loosen the grip of the film on the dice.

[0042] DRAM IC dice identified as good by their electronic wafer map are then each picked by automated equipment from their sawed wafer and its associated film in a die attach step 64 and placed on an epoxy-coated bonding site of one lead frame in a strip of interconnected lead frames, while DRAM IC dice identified as bad are discarded into the scrap bin 42. In addition, DRAM IC's 44 that have been diverted from COB and flip-chip manufacturing process flows enter the assembly process 40 and are also placed on an adhesive-coated bonding site of one lead frame in a lead frame strip. These diverted DRAM IC's 44 will be described in more detail below with respect to FIG.'s 4A and 4B. The adhesive attaching the good DRAM IC dice to their lead frames is then cured, if required, in a cure step 66, and the attached dice are wire bonded to their lead frames using high-speed bonding equipment in a wire bond step 68.

[0043] Once wire bonded, DRAM IC dice and their lead frames continue the assembly process 40 by being formed into DRAM IC packages using a hot thermosetting plastic encapsulant injected into a mold in an overmold step 70. DRAM IC packages are then cured in a further cure step 72 to set their plastic encapsulant. After encapsulation and curing, leads of the

lead frames projecting from the packages may be dipped in a cleansing chemical bath in a de-flash process 74 and then may be electroplated with a lead/tin finish if they are not already plated. Finally, connections between the lead frames of different DRAM IC packages are then cut in a singulate step 76 to separate the packages into discrete DRAM IC devices.

[0044] In another embodiment of the present invention shown in FIG. 4A, an inventive COB or flip-chip process 80 for manufacturing DRAM SIMM's begins with DRAM IC's being fabricated in a fabrication step 82 on the surface of a semiconductor wafer 84. It will be understood by those having skill in the field of this invention that the present invention is applicable to any IC devices, including SRAM IC's, SDRAM IC's, processor IC's, and modules using such IC devices, such as DIMM's, RIMM's, SO-RIMM'S, PCMCIA's, COB's, BOC's, and other MCM's. It will also be understood that although the present invention will be described below in the context of both a COB process and a flip-chip assembly process, the present invention is applicable to any IC assembly process, including, for example, Tape-Automated Bonding (TAB) processes, wafer scale processes including packaging, partial wafer scale processes including packaging, etc. It should be further understood that the present invention relates to any type IC that has been singulated by any type singulation process or apparatus, such as wafer saw singulation, laser apparatus singulation, laser/water apparatus singulation (cool laser singulation), water jet apparatus singulation, etc.

[0045] Once fabricated, the DRAM IC's are electronically probed in a probe step 86 to determine whether they are good or bad, and if any DRAM IC's are found to be bad, an attempt is made to repair the IC's by replacing nonfunctional rows or columns in the IC's with spare rows or columns. The locations of bad DRAM IC's on a wafer 84, along with the locations of any good DRAM IC's on the wafer 84, are stored in a computer in an electronic wafer map in association with repair data 48 identifying spare rows and columns still available in each of the DRAM IC's after any repairs performed at the probe step 86.

[0046] During the probe step 86, DRAM IC's fabricated on the wafers 84 are programmed in the manner described above with a fuse identification (ID) unique to each IC. The fuse ID for each DRAM IC is then stored in association with the repair data 48 for that IC.

The fuse ID may identify, for example, a wafer lot ID, the week the DRAM IC's were fabricated, a wafer ID, a die location on the wafer, and a fabrication facility ID.

[0047] It will be understood, of course, that the present invention includes within its scope IC's having any ID code, including those having fuse ID's. It will also be understood that the IC's may be programmed with their fuse ID's at steps in the manufacturing process 80 other than the probe step 86.

[0048] After being probed and, if necessary, repaired, DRAM IC's enter an assembly process 90 in which good IC's are assembled into panels of physically interconnected DRAM SIMM's, as will be described in more detail below with respect to FIG. 4B, while bad IC's are discarded in a scrap bin 92. In addition, DRAM IC's 44 in which so many spare rows and columns have been used at the probe step 86 to effect repairs that the IC's 44 fall below a minimum threshold of repairability are diverted from the COB or flip-chip process 80 for use in the standard assembly process 40 of FIG.'s 3A and 3B. Although a "minimum threshold of repairability" can be set at any level, it might be set, for example, at a level at which statistically the available spare rows and columns in a DRAM IC would only be able to effect repairs in an unacceptably low percentage (e.g., 50%) of cases of failures. Thus, the diverted DRAM IC's 44 typically include those IC's that have exhausted their spare rows and columns in repairs at the probe step 86 and those IC's that have some, but not enough, spare rows and columns left after being repaired at the probe step 86.

[0049] The present invention thus prevents DRAM IC's that would be repairable in few or none of the possible cases of failure from being assembled into DRAM SIMM's and other MCM's, and thus prevents the waste of time and resources associated with scrapping or reworking MCM's into which such IC's have traditionally been assembled.

[0050] After the assembly process 90, panels of DRAM SIMM's are tested in an opens/shorts test 96. There, the fuse ID of each DRAM IC in each DRAM SIMM is automatically read and correlated with the repair data 48. It should be understood that although the fuse ID's of DRAM IC's in the process 80 are typically read electronically, they may also be read optically if the fuse ID's consist of "blown" laser fuses that are optically accessible. It

should also be understood that the fuse ID's of DRAM IC's may be read at steps in the process 80 other than the opens/shorts test 96.

[0051] When the manufacturing process 80 is a COB process, panels of DRAM SIMM's having COB IC dice that pass the opens/shorts test 96 proceed to an encapsulation step 98 so the dice can be encapsulated using an overmold, hard cover, or glob top. Alternatively, when the manufacturing process 80 is a flip-chip process, panels of DRAM SIMM's having flip-chip IC dice that pass the opens/shorts test 96 may have their dice encapsulated at the encapsulation step 98 using an underfill followed by an overmold, hard cover, or glob top. As will be described in more detail below, alternatively, the flip-chip IC dice may be encapsulated after burn-in and test procedures. The disposition of panels of DRAM SIMM's having IC dice that fail the opens/shorts test will be described in more detail below.

[0052] Panels of DRAM SIMM's having either COB or flip-chip IC dice, including those panels of SIMM's having flip-chip IC dice that were not encapsulated at the encapsulation step 98, are then singulated into discrete DRAM SIMM's at a singulation step 100 by, for example, a water jet or a shear press. This singulation step 100 may, for example, divide a "ten" panel of ten physically attached DRAM SIMM's into ten discrete DRAM SIMM's.

[0053] After singulation, DRAM SIMM's having encapsulated IC dice are tested again in an additional opens/shorts test 102 to check for problems caused by the encapsulation step 98. DRAM SIMM's having encapsulated dice that pass this additional opens/shorts test 102, as well as DRAM SIMM's having dice that were not encapsulated, then proceed on in the manufacturing process 80 to burn-in testing 104 and back-end testing 106. The disposition of those DRAM SIMM's having encapsulated IC dice that fail the additional opens/shorts test 102 will be described in more detail below. The fuse ID's of the IC dice in the DRAM SIMM's may also be automatically read at this additional opens/shorts test 102.

[0054] After the burn-in and test procedures 104 and 106, DRAM SIMM's having un-encapsulated flip-chip IC dice that pass the procedures 104 and 106 proceed on in the process 80 to an optional cover step 108 so their dice may be covered with an overmold, hardcover, or glob top. Dice covered in this manner are then checked in a further opens/shorts test 108 for problems caused by their being covered, and DRAM SIMM's having dice that pass this further test are then

typically shipped in a shipping step 110 to customers. DRAM SIMM's having encapsulated IC dice that pass the burn-in and test procedures 104 and 106 skip this covering and final opens/shorts test step 108 and proceed to the shipping step 110. Of course, the fuse ID's of the IC dice in the DRAM SIMM's tested at any of the burn-in, back-end test, and opens/shorts test procedures 104, 106, and 108 may be automatically read at any one or all of those tests.

[0055] DRAM SIMM's having IC dice that fail any of the opens/shorts, burn-in, and test procedures 96, 102, 104, 106 and 108 proceed to repair 112. Those DRAM SIMM's having DRAM IC dice that do not have enough available spare rows and columns to effect repairs, and thus are unrepairable, are identified as such when their repair data 48 is accessed at any one of the opens/shorts, burn-in, and back-end tests 96, 102, 104, 106, and 108, and these SIMM's proceed directly to rework (described below) or a scrap bin 114 without the need to query them. Of course, DRAM SIMM's having DRAM IC dice identified by their repair data 48 as being repairable are repaired, typically by replacing nonfunctional rows and columns with spare rows and columns in the same manner as described above. After being repaired, these DRAM SIMM's then reenter the manufacturing process 80 just prior to the opens/shorts, burn-in, or test procedures 96, 102, 104, 106 or 108 they failed.

[0056] Those DRAM SIMM's that are reworkable by replacing one or more non-functioning IC dice proceed through a Known Good Die (KGD) process in which a DRAM KGD (*i.e.*, a burned-in, fully tested, fully functional DRAM) replaces the non-functioning IC dice on the SIMM's in a replacement step 116. The KGD repairs are then tested in a repair step 118, and if the repairs are successful, the repaired DRAM SIMM's reenter the manufacturing process 80 just prior to the back-end test procedures 106. If the repairs are not successful, the DRAM SIMM's may return to the repair step 112 to be reworked again or, if they are not reworkable, to be scrapped in the scrap bin 114.

[0057] As stated above, the assembly process 90 of FIG. 4A is shown in more detail in FIG. 4B. In the process 90, probed and repaired semiconductor wafers enter a wafer saw step 120 and are mounted on an adhesive film. The film may be any one of a wide variety of adhesive films used for this purpose, including, for example, a special high-adhesion U.V. film. Without cutting the film, DRAM IC's are then sawed from their wafer into discrete DRAM IC

dice using high-speed precision dicing equipment. DRAM IC dice that are mounted on the special high-adhesion U.V. film are then exposed to U.V. light in an optional U.V. exposure step 122 to loosen the grip of the film on the dice.

[0058] IC dice identified as good by their electronic wafer map are then each picked by automated equipment from their sawed wafer and its associated film at an attachment step 124. If the assembly process 90 is a flip-chip process, multiple picked dice are then flipped and directly attached at their active, frontside surfaces to a panel of PCB's or other substrates to form, for example, DRAM SIMM's. If the assembly process 90 is a COB process, multiple picked dice are directly attached at their inactive, backside surfaces to an adhesive-coated bonding site of a panel of PCB's or other substrates to form, for example, DRAM SIMM's. DRAM IC's identified as bad are discarded into the scrap bin 92, while DRAM IC's 44 that have used so many of their spare rows and columns in repairs at the probe step 86 that they fall below the minimum threshold of repairability are diverted to the standard assembly process 40 of FIG.'s 3A and 3B. Panels of DRAM SIMM's are then cured at a cure step 126. If the assembly process 90 is a COB process, the panels may be plasma cleaned in an optional plasma cleaning step 128, if necessary, and the COB IC dice are then wire bonded at a wire bond step 130 to their DRAM SIMM's using high-speed bonding equipment. DRAM SIMM's then proceed to the opens/shorts test 96 described above with respect to FIG. 4A.

[0059] Although the present invention has been described with reference to particular embodiments, the invention is not limited to these embodiments. For example, while the various steps of these embodiments have been described as occurring in a particular order, it will be understood that these steps need not necessarily occur in the described order to fall within the scope of the present invention. Thus, the invention is limited only by the appended claims, which include within their scope all equivalent methods that operate according to the principles of the invention as described.